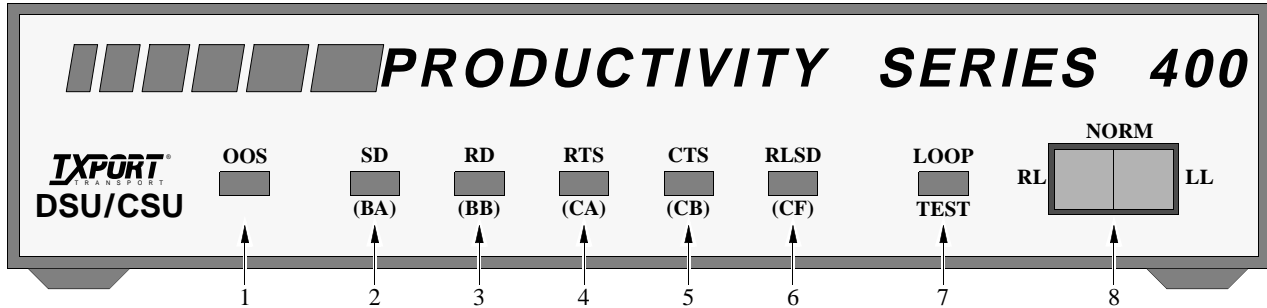


TxPORT 400 Front Panel



Front Panel Description

1	OOS: This three color Out Of Service LED indicates the DDS loop receiver's operating status as follows: Green: Indicates DDS signal at the receiver (either customer data or zero suppression). Amber: Indicates DDS signal is still present, but received data is idle or out of service. Red: Indicates an insufficient signal for the DDS receiver to operate properly.
2	SD: This green Send Data LED illuminates when the data lead is a mark and is Off when the data lead is a space. Therefore, the LED will vary from full intensity to Off depending on the relative number of marks and spaces.
3	RD: This green Receive Data LED illuminates when the data lead is a mark and is Off when the data lead is a space. Therefore, the LED will vary from full intensity to Off depending on the relative number of marks and spaces.
4	RTS: This green Request To Send LED illuminates when circuit CA is in the On state at the DSU interface.
5	CTS: This green Clear To Send LED illuminates when circuit CB is in the On state at the DSU interface.
6	RLSD: This green Receive Line Signal Detector LED illuminates when circuit CF is in the On state at the DSU interface.
7	TEST: This amber LED remains illuminated if the unit is in a test mode, either by manually depressing the loop switch or by receipt of a test command from the facility. The LED turns red or green at the end of a V.54 test indicating the pass or fail state of the BERT.
8	Test Switch: This 3-position switch is used as follows: The LL position places the unit in a local loop mode. Data from the DTE is looped back to the DTE. Data from the network is looped back to the network. The RL position initiates an automated V.54 remote loop and BERT sequence of assigned data channels. The TEST LED will illuminate green if the test is successful (the far end unit loops and returns the data error free with the V.54 code). If errors are detected, the TEST LED will illuminate red. The NORM position deactivates the loop codes for normal operation.

Specifications

Network Interface

Line Rate: 2.4, 4.8, 9.6, 19.2, 28, 38.4, 56, and 64 kbps
 Line Code: AMI
 Line Impedance: balanced 135 Ω
 Input Signal: +1 to -40 dB (ALBO)
 Output Signal: 3.0 V ($\pm 15\%$) base-peak into 135 Ω
 1.5 V ($\pm 15\%$) at the 9.6 kbps line rate
 Line Protection: 1000 V lightning, input/output

Power

AC Power: 115 VAC ($\pm 10\%$), 150 mA max, 20 Watts, 73 BTU max.
 Connection: 5-foot power cord

Mechanical

Mounting: Desktop or wall

Dimensions:
 Height: 1.75 inches (4.45 cm)
 Wide: 6.8 inches (17.27 cm)
 Depth: 10.5 inches (26.67 cm)
 Weight: 2 pounds (0.91 kg)

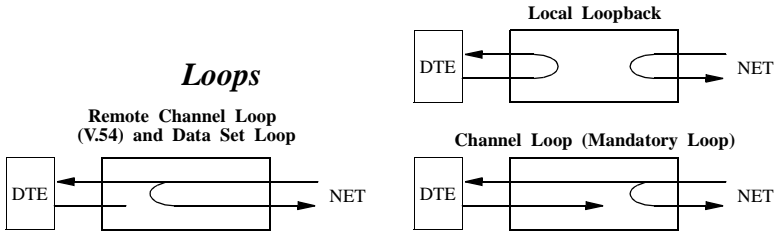
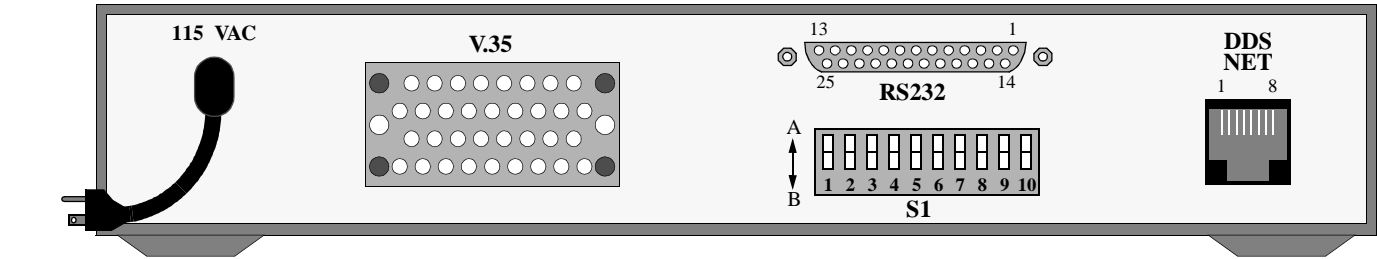
Industry Standards

FCC Compliance: Part 15 Subpart B, Class A, Part 68
 U.S. Safety: UL 1459
 Canadian Safety: CSA C22.2 No. 225-M90
 IC: CS03

Environmental

Operating Temp: 0° to 50° C (32° to 122°F)
 Storage Temp: -20° to 85° C (-4° to 185°F)
 Humidity: 95% max (non-condensing)

TxPORT 400 Rear Panel



DDS NET Pinout

1	Data Out R
2	Data Out T
3-6	Not Used
7	Data In T1
8	Data In R1

Switch S1

- Channel Bitrate Select:** These 3 positions select the channel bit rate (refer to the table on the right). The RTS to CTS delays are multiplied by 2 when S1-10 is in the B position.
- Line Clock:** This position selects either an internal clocking source or a loop timing source from the received data.
- Internal Clock:** This position selects either the DSU external clock input or the crystal oscillator as the clocking source. It is applicable only if S1-4 is in the B position.
- V.54 Loop Operation:** This position enables or inhibits V.54 loop operation.
- Data Polarity:** This position determines whether data bits are inverted. In the A position, marks equal pulses. In the B position, spaces equal pulses. Receipt of OOF, OOS, idle, or loop codes forces the DSU data to all marks (A position) or spaces (B position).
- Circuit Assurance:** On allows the status of CF (receive line signal detector) and CA (request to send) to control the output CB (clear to send). If either CA or CF is Off (position A), CB is Off. If CA and CF are On (position 'B'), CB is On.
- RTS/CTS Control:** In the B position, CTS is forced On regardless of the RTS input status. In the A position, delays are determined by S1-10.
- RTS -> CTS Delay:** In the A position, the RTS to CTS delay is as shown in the bit rate table of the diagram. In the B position, the delays shown are multiplied by two.

Rate (kbps)	S1-1	S1-2	S1-3	RTS to CTS Delay
2.4	B	B	B	8 ms
4.8	A	B	B	4 ms
9.6	B	A	B	2 ms
19.2	A	A	B	1 ms
28	B	B	A	.8 ms
38.4	A	B	A	.5 ms
56	B	A	A	.4 ms
64	A	A	A	.3 ms

A	n/a	Network (slave)
B	A	Master
B	B	External

A	V.54 Loop Enabled
B	V.54 Loop Inhibited
A	Data Polarity Normal
B	Data Polarity Inverted
A	Circuit Assurance On
B	Circuit Assurance Off
A	RTS/CTS Control On
B	RTS/CTS Control Off
A	RTS->CTS Delay X 2
B	RTS->CTS Delay Normal

Note: The symbol '└─' indicates that the switch pointed to is not functional unless the opposite end of the arrow is in the position shown. For example, S1-5 is not functional unless S1-4 is in the B position.

V.35 and RS-232 Interface

Ckt.	V.35	RS-232	Signal Name - Function	(Note: all other pins are open)	DCE
101	A	1	Frame Ground	- This circuit is used to terminate shields.	Gnd
102	B	7	Signal Ground	- This circuit is used as the return reference for unbalanced signals.	Gnd
103	P/S	2	Transmit Data	- This input is used for synchronous TD from the DTE. It is transmitted on the DDS side.	In
104	R/T	3	Receive Data	- This output is the data decoded from the incoming DDS receive data.	Out
105	C	4	Request To Send	- This input is a control line from the DTE indicating data is to be transmitted. When RTS is On (space), the data transmitter, the zero suppression circuitry, and the CTS are enabled. When RTS is Off, the transmitter sends idle code and the CTS is forced Off.	In
106	D	5	Clear To Send	- This output is a DCE response, indicating that either RTS is On or S1-8, position B, is forcing RTS ON. When S1-7 is in position B, RTS and RLSD must be On for CTS to be On.	Out
107	E	6	Data Set Ready	- This output is On when the unit is not in a test mode (other than a V.54 test).	Out
109	F	8	Data Carrier Detect	- This output is On when the correct data or zero suppression code is being received and DSR is On. It is Off when either DSR is Off, the DDS receiver has lost sufficient signal to operate for at least one second, or the receiver has received OOS, OOF, idle, or loop codes for about 20 U.I.	Out
113	U/W	24	External Transmit Clock	- This is the synchronous transmit clock input from the DTE. When both S1-3 and S1-4 are in the B position, this clock controls the frequency of the DDS transmit clock and clocks circuit 103 (TD). When either S1-3 or S1-4 is in the A position, this input has no effect on DDS operation.	In
114	Y/AA	15	Transmit Clock	- This output is supplied by the DCE as an external DTE timing source. It is generated from the internal data clock or the far end transmit data. Not available when S1-3 and S1-4 are in the B position.	Out
115	V/X	17	Receive Clock	- This clock output is the timing for the RD and is always used to time the receive data. This clock is always derived from the DDS receive data.	Out
142	K	25	Test Mode	- This output is On when the unit is in the Test/Loop mode.	Out

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